AMENDMENTS TO THE CLAIMS

Please amend the claims as shown below:

Claim 1 (Currently Amended). A method of forming a differential transistor comprising:

forming an enhancement mode transistor of a first conductivity type having a source coupled to a source of a depletion mode transistor of a second conductivity type; ~~and~~

forming a threshold voltage of the enhancement mode transistor so that an absolute value of the threshold voltage of the enhancement mode transistor is no greater than an absolute value of a threshold voltage of the depletion mode transistor;

forming a second depletion mode transistor having a gate and a source coupled to receive a voltage from a voltage source and having a drain coupled to a gate of one of the enhancement mode transistor or the depletion mode transistor;

forming a third depletion mode transistor having a drain coupled to a drain of the depletion mode transistor and having a gate and a source coupled to a gate of one of the enhancement mode transistor or the depletion mode transistor.

2 (Cancelled).

3 (Cancelled).

4 (Cancelled).

5 (Cancelled).

6(Currently Amended). ~~The method of claim 5 wherein coupling the drain of the enhancement mode transistor to the first signal includes~~

A method of forming a differential transistor comprising:

forming an enhancement mode transistor of a first conductivity type having a source coupled to a source of a depletion mode transistor of a second conductivity type;

forming a threshold voltage of the enhancement mode transistor so that an absolute value of the threshold voltage of the enhancement mode transistor is no greater than an absolute value of a threshold voltage of the depletion mode transistor;

coupling a gate of the enhancement mode transistor to a gate of another enhancement mode transistor, coupling a drain of the depletion mode transistor to a voltage return, coupling a gate of the depletion mode transistor to a gate and a drain of another depletion mode transistor and to a drain of the another enhancement mode transistor, coupling a source of the another enhancement mode transistor to receive a voltage from a voltage source; and

coupling ~~the~~ a drain of the enhancement mode transistor to a first terminal of a resistor and to a signal input of a microprocessor, and coupling a second terminal of the resistor to receive the voltage from the voltage source.

7(Currently Amended). The method of claim ~~5~~6 further including coupling a source of the another depletion mode transistor to the voltage return.

8(Currently Amended). ~~The method of claim 5 further including~~
A method of forming a differential transistor comprising:

forming an enhancement mode transistor of a first conductivity type having a source coupled to a source of a depletion mode transistor of a second conductivity type;

forming a threshold voltage of the enhancement mode transistor so that an absolute value of the threshold voltage of the enhancement mode transistor is no greater than an absolute value of a threshold voltage of the depletion mode transistor;

coupling a drain of the enhancement mode transistor to receive a first signal;

coupling a gate of the enhancement mode transistor to a gate of another enhancement mode transistor, coupling a drain of the depletion mode transistor to receive a second signal, coupling a gate of the depletion mode transistor to a gate and a drain of another depletion mode transistor and to a drain of the another enhancement mode transistor, coupling a source of the another enhancement mode transistor to receive a voltage from a voltage source; and

coupling a source of the another depletion mode transistor to a drain of a lower output transistor and coupling a source of the lower output transistor to ~~the~~ a voltage return.

9(Currently Amended). ~~The method of claim 4 further including~~

A method of forming a differential transistor comprising:

forming an enhancement mode transistor of a first conductivity type having a source coupled to a source of a depletion mode transistor of a second conductivity type; and

forming a threshold voltage of the enhancement mode transistor so that an absolute value of the threshold voltage of the enhancement mode transistor is no greater than an absolute value of a threshold voltage of the depletion mode transistor; and

coupling the drain of the depletion mode transistor to receive a first signal, coupling a gate of the depletion mode transistor to a gate of another enhancement mode transistor, coupling the drain of the enhancement mode transistor to a voltage return, coupling a gate of the enhancement mode transistor to a drain of another depletion mode transistor and to a drain of the another enhancement mode transistor, coupling a source of the another depletion mode transistor to a gate of the another depletion mode transistor, and coupling a source of the

another enhancement mode transistor to receive a voltage from a voltage source.

10(Original). The method of claim 9 wherein coupling the drain of the depletion mode transistor to receive the first signal includes coupling the drain of the depletion mode transistor to a first terminal of a resistor and to a signal input of a microprocessor and coupling a second terminal of the resistor to receive the voltage from the voltage source.

11(Original). The method of claim 9 further including coupling the source of the another depletion mode transistor to the voltage return.

12(Original). The method of claim 9 further including coupling a source of the another depletion mode transistor to a drain of a lower output transistor and coupling a source of the lower output transistor to the voltage return.

13 (Cancelled).

14 (Cancelled).

15 (Cancelled).

16(Currently Amended). ~~The differential transistor of claim 13 further including~~

A differential transistor comprising:

a depletion mode MOS transistor of a first conductivity type having a first source, a first drain, a first gate, and a first threshold voltage;

an enhancement mode MOS transistor of a second conductivity type having a second source connected to the first source, having a second drain, having a second gate, and having a second threshold voltage having an absolute value that is less than an absolute value of the first threshold voltage, wherein the first drain is coupled to a first terminal of a resistor and to a signal input of a microprocessor and wherein a second terminal of the resistor is coupled to a voltage source.

17. The differential transistor of claim 16 further including the second drain coupled to a voltage return.

18(Currently Amended). ~~The differential transistor of claim 13 further including~~

A differential transistor comprising:

a depletion mode MOS transistor of a first conductivity type having a first source, a first drain, a first gate, and a first threshold voltage;

an enhancement mode MOS transistor of a second conductivity type having a second source connected to the first source, having a second drain, having a second gate, and having a second threshold voltage having an absolute value that is less than an absolute value of the first threshold voltage, the second drain coupled to a first terminal of a resistor and to a signal input of a microprocessor, a second terminal of the resistor coupled to a voltage source, and the first drain coupled to a voltage return.

19(Cancelled).

20(Cancelled).